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JC542 U.S. PTO 09/618622 07/18/00

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Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Case Docket No. 0325.00377
Date: July 18, 2000

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): I-Teh Sha, Kuang-Yu Chen and Albert Chen

For: ADAPTIVE SPREAD SPECTRUM

Enclosed are:

1. X Specification (15 pages); Claims (5 pages); Abstract (1 page)

2. X 5 sheets of formal drawings.

3. X Oath or Declaration Total Pages 3
   a. X Newly executed (original or copy)
   b. ___ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Item 5 completed)
   c. ___ Copy of Revocation of Previous Power

4. ___ Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

5. ___ If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

___ Continuation _____ Divisional _____ Continuation-in-part (CIP)
of prior application no.: _____

6. X An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form 1595.

7. ___ A PTO Form 1449 with a copy of the references not previously cited.

8. X Return Receipt Postcard

9. ___ Other:

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Fee	Amount
Basic Fee	--	--	--	$690.00
Total Claims	20	0	x $ 18.00	$ 0.00
Indep. Claims	3	0	x $ 78.00	$ 0.00
Mult. Dep. Claims			$260.00	$ 0.00

SUB-TOTAL $690.00

__ SMALL ENTITY STATUS (divide SUB-TOTAL by two) ..... $ ____

X Assignment Recordal Fee ($40.00) ..... $ 40.00

TOTAL $730.00

X A check in the amount of $730.00 to cover the filing fee is enclosed.

X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

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PATENT TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL561050675US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on July 18, 2000.

By: Mary Donna Berkley
Mary Donna Berkley

Respectfully submitted,

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Attorney Docket No.: 0325.00377

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ADAPTIVE SPREAD SPECTRUM

Cross Reference to Related Applications

The present application may relate to co-pending application Serial No. 09/_____ (Attorney Docket No. 0325.00378), filed concurrently, which is hereby incorporated by reference in its entirety.

Field of the Invention

The present invention relates to a method and/or architecture for generating a spread spectrum clock generally and, more particularly, to a method and/or architecture for generating an adaptive spread spectrum clock.

Background of the Invention

Electronic devices must meet maximum electromagnetic interference (EMI) radiation limits as specified by the United States Federal Communications Commission (FCC) and other comparable regulatory agencies in other countries. New FCC requirements call for personal computer (PC) motherboards to be able to pass

electromagnetic interface (EMI) tests "open box," so manufacturers will not be able to rely on the shielding provided by the case in meeting EMI requirements.

An EMI suppression-enabled clock integrated circuit (IC) can reduce the system radiated EMI. The reduction in radiated EMI can result in dramatic cost savings for the system. Conventional techniques for reducing EMI include ground planes, filtering components, shielding, and spread spectrum modulated system clocks.

In the spread spectrum technique, instead of concentrating all of a frequency reference's energy on a single frequency, the energy is spread out by modulating the frequency. The modulation results in the energy being spread over a frequency range, instead of being concentrated on one particular frequency. Since the FCC and other regulatory bodies are concerned with peak emissions, not average emissions, the reduction in peak energy due to spread spectrum modulation will help a product meet FCC requirements.

Referring to FIG.1, a block diagram of a circuit 10 illustrating a conventional phase lock loop based spread spectrum clock generator is shown. The circuit 10 generates a signal OUT in response to a reference signal REF. The circuit 10 comprises a

phase detector 12, a charge pump 14, a low pass filter 16, a linear voltage controlled oscillator (VCO) 18, a feedback divider 20 and a spread spectrum circuitry block 22. The phase detector 12 has a first input that receives a reference signal REF and a second input that receives a feedback signal FEEDBACK. An output of the phase detector 12 presents a pump signal PUMP to an input of the charge pump 14. The charge pump 14 generates a control signal VIN in response to the signal PUMP. The signal VIN is filtered by a low pass filter 16 and presented to an input of the linear VCO 18. The linear VCO 18 generates a signal OUT in response to the signal VIN. The signal OUT has a frequency that is linearly dependant upon a voltage level of the signal VIN. The signal OUT is presented to an input of the feedback divider 20. The feedback divider 20 generates the signal FEEDBACK in response the signal OUT and a control signal SSM. The signal FEEDBACK is presented to an input of the spread spectrum circuitry block 22. The spread spectrum circuitry block 22 generates the signal SSM in response to the signal FEEDBACK and a set of ROM codes 24. The frequency of the signal OUT is modulated in response to the signal SSM.

Referring to FIG. 2, a line graph illustrating the frequency of the signal OUT versus the voltage level of the signal

VIN is shown. The frequency of the signal OUT is linearly related to the voltage level of the signal VIN. Changes in the frequency of the signal OUT are related to changes in the voltage level of the signal VIN by a constant value.

The set of ROM codes 24 of a conventional digital spread spectrum clock generator are optimized for a particular frequency. For good performance, a conventional spread spectrum clock generator requires a separate set of ROM codes for each frequency at which the spread spectrum clock generator will operate. In order to get the best EMI reduction, every applied frequency needs a unique set of ROM codes. A full range of applied frequency can vary from 50MHz to 170MHz. In order to cover the full range using conventional spread spectrum clock generating devices, at least 5 devices are required. Each of the devices is configured to operate over a 10 MHz portion of the full range. However, the best performance is at the optimized frequency of the ROM codes of each device. The performance of the devices at other than optimized frequencies will be compromised.

A set of spread spectrum ROM codes occupies a large portion of a spread spectrum device. Multiple sets of ROM codes requires large amounts of space. Without multiple sets of ROM

codes, the effectiveness of spread spectrum modulation is compromised as frequency changes.

Referring to FIGS. 3a-3d, oscilloscope traces illustrating degradation of the spread spectrum modulation of the signal OUT at various frequencies. As the frequency of the signal OUT changes, modulation of the frequency of the signal OUT varies from an ideal profile (i.e., FIG. 3b). FIG. 3b illustrates the signal OUT having a mean frequency of 79 MHz. When the signal OUT has a mean frequency of 79 MHz, modulation of the signal FOUT follows an ideal profile for spread spectrum modulation. FIG. 3a illustrates changes in the modulation profile when the signal OUT has a mean frequency of 48 MHz. FIG. 3c illustrates the signal OUT having a mean frequency of 107 MHz. When the signal OUT has a mean frequency of 107 MHz, modulation of the signal OUT is similar to a triangle waveform. Referring to FIG. 3d, as the mean frequency of the signal OUT increases to 149 MHz, modulation of the signal OUT becomes sinusoidal.

Another conventional approach that uses a single set of ROM codes for multiple frequencies is to adjust the bandwidth of the spread spectrum clock generator using an external low pass filter. The components of the external filter must be changed to

compensate for each change in frequency. However, the external low pass filter provides very limited improvement.

A spread spectrum clock generator that uses a single set of ROM codes, requires no adjustment, and could generate any frequency in a wide range of frequencies, would be desirable.

Summary of the Invention

The present invention concerns an apparatus comprising a circuit that may be configured to generate a spread spectrum clock signal. The circuit may comprise a voltage controlled oscillator that may have an automatically controlled gain.

The objects, features and advantages of the present invention include providing a method and/or architecture for generating an adaptive spread spectrum clock that may (i) provide all frequency spreading in one device, (ii) spread spectrum modulate any frequency of a continuous range, (iii) require only one set of ROM codes and/or (iv) automatically adjust a gain of a voltage controlled oscillator (VCO) in response to frequency changes.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a conventional spread spectrum PLL;

FIG. 2 is a line graph illustrating a transfer function of a linear voltage controlled oscillator of FIG. 1;

FIGS. 3a-3d are oscilloscope traces illustrating operation of the circuit 10 of FIG. 1;

FIG. 4 is a block diagram of a preferred embodiment of the present invention;

FIG. 5 is a more detailed block diagram of a preferred embodiment of the present invention;

FIG. 6 is a line graph illustrating an example operation of a voltage controlled oscillator of FIGS. 4 and 5;

FIG. 7 is a flow chart illustrating a process for determining a gain curve in accordance with the present invention; and

FIGS. 8a-8d are graphs illustrating an example operation of a preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 4, a block diagram of a circuit 100 illustrating a preferred embodiment of the present invention is shown. The circuit 100 may be implemented, in one example, as a spread spectrum clock generating circuit for use in analog applications. The circuit 100 may have an input 102 that may receive a reference signal (e.g., REF) and an output 104 that may present a clock signal (e.g., FOUT). The signal FOUT may be, in one example, a spread spectrum clock signal that has a mean frequency determined by the frequency of the signal REF. The circuit 100 may provide optimized spread spectrum modulation over a wide range of frequencies of the signal REF.

The circuit 100 may comprise a circuit 106 and a circuit 108. The circuit 106 may be, in one example, a control circuit for controlling the frequency of the signal FOUT. The circuit 108 may be implemented, in one example, as a voltage controlled oscillator (VCO) having an automatically controlled gain (e.g., Kvco). In one example, the circuit 108 may have a non-linear gain. The circuit 106 may receive the signal REF and the signal FOUT. The circuit 106 may have an output that may present a signal (e.g., VIN) to an input of the circuit 108. The signal VIN may be a control signal.

The signal VIN may have a voltage level that may vary in response to the signals REF and FOUT. The circuit 108 may be configured to generate the signal FOUT in response to the signal VIN.

Referring to FIG. 5, a more detailed block diagram of the circuit 100 is shown. The circuit 106 may comprise, in one example, a phase detector 110, a charge pump circuit 112, a low pass filter 114, a feedback divider 116 and a spread spectrum circuitry block 118. The signal REF may be presented to a first input of the phase detector 110. A feedback signal (e.g., FEEDBACK) may be presented to a second input of the phase detector 110. The phase detector 110 may have an output that may present a signal (e.g., PUMP) to an input of the charge pump 112. The charge pump 112 may have an output that may present a signal to an input of the low pass filter 114. The low pass filter 114 may have an output that may present the signal VIN. The circuit 108 may be configured to generate the signal FOUT in response to the signal VIN.

The signal FOUT may be presented to a first input of the feedback divider 116. A control signal (e.g., SSM) may be presented to a second input of the feedback divider 116. The feedback divider may have an output that may present the signal

FEEDBACK in response to the signals FOUT and SSM. The signal FEEDBACK may be presented to an input of the spread spectrum circuitry block 118. The spread spectrum circuitry block 118 may comprise a set of spread spectrum ROM codes 120. The set of ROM codes may have been optimized for a particular mean frequency of the signal FOUT according to predetermined criteria. The spread spectrum circuitry block 118 may be configured to generate the signal SSM in response to the signal FEEDBACK and the set of ROM codes 120.

Referring to FIG. 6, a line graph illustrating an example relationship between the frequency of the signal FOUT and the voltage level of the signal VIN for the circuit 108 is shown. The gain Kvco of the circuit 108 may provide a non-linear relationship between the frequency of the signal FOUT and the voltage level of the signal VIN. In one example, the non-linear relationship may be represented as a parabolic function. However, the gain Kvco may be implemented accordingly with other second order or higher polynomial functions to meet the design criteria of a particular application. The gain Kvco may be, in one example, a function of the frequency of the signal FOUT (e.g., Kvco(f)). The function Kvco(f) may be determined, in one example, using a computer program

or other suitable means for simulating behavior of the circuit 100 at various frequencies and various gains.

Referring to FIG. 7, a flow chart illustrating a process for determining a gain function (curve) of the circuit 108 in accordance with the present invention is shown. The process of determining the gain function of the circuit 108 may have an initial step of determining input requirements for the set of spread spectrum ROM codes of the spread spectrum circuitry 118 and resistance and capacitance values of components in the low pass filter 116 (e.g., R1, C1, C2 and CP(T), block 202). When the initial conditions have been determined, the next step may be to select an operating frequency for the circuit 108 (e.g., block 204). An iterative process may be used, in one example, to determine a best value for the gain of the circuit 108 for the selected operating frequency (e.g., Kvco(f)).

A first step of the iterative process may be to set the gain of the simulated circuit 108 (e.g., Kvco(i)) to a minimum value (e.g., Kvco(min), block 206). Next, a model of the spread spectrum performance of a phase lock loop (PLL) implemented with the circuit 108 may be set up (e.g., block 208). Behavior of the PLL may be simulated for a number of modulation cycles. In one

example, ten modulation cycles may be simulated (e.g., block 210). When the number of modulation cycles have been simulated, an accumulated error deviation from an ideal modulation profile may be calculated (e.g., block 212). After determining the accumulated error deviation, a check may be made to see whether a maximum gain (e.g., Kvco(max)) has been reached (e.g., block 214). If the maximum gain Kvco(max) has not been reached, then the gain parameter may be incremented by a predetermined delta gain (e.g., ΔKvco, block 216) and another iteration performed. The process may be repeated until the range of gains Kvco(min)-Kvco(max) may have been simulated, as indicated by the arrow to the block 208.

When the maximum gain Kvco(max) has been reached, the process may branch to a determination of a particular gain Kvco(i) that generally produced a least amount of error (e.g., block 218). After determining the gain Kvco(i) a check may be made to see whether a maximum frequency (e.g., f(max)) for the particular application may have been reached (e.g., block 220). If the maximum frequency f(max) has not been reached, a next frequency may be selected and the process may be repeated for the next frequency. If the maximum frequency f(max) has been reached, the process may branch to a termination stage (e.g., block 220). The termination

stage may be entered, in one example, when a gain Kvco(i) has been determined for the frequencies in a predetermined range (e.g., 50MHz-170MHz).

The function performed by the flow diagram of FIG. 7 may be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will also be apparent to those skilled in the relevant art(s).

The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a computer to perform a process in accordance with the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disk, optical disk, CD-ROM, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, Flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions.

Referring to FIGS. 8a-8d, oscilloscope traces illustrating the signal FOUT in accordance with the present

invention. The signal FOUT is generally illustrated having frequencies similar to the signal OUT as illustrated in the FIGS. 3a-3d. A comparison of the FIGS. 3a-3d to the FIGS. 8a-8d generally shows that the present invention may provide improved spread spectrum modulation over a wider frequency range than a conventional spread spectrum clock generator.

The present invention may provide a digital spread spectrum apparatus and/or method with analog spread spectrum capabilities. The present invention may comprise, in one example, a voltage controlled oscillator having an automatically controlled gain and a set of ROM codes. The set of ROM codes may be optimized for a particular frequency. When a selected VCO frequency is higher than the optimized frequency, the gain of the VCO may be adjusted higher. When the selected VCO frequency is lower than the optimized frequency, the gain of the VCO may be adjusted lower. A computer program may be used to model a spread spectrum clock generator in accordance with the present invention. The computer program may determined a gain curve that may describe the gain of the VCO as a function of output frequency. The VCO gain curve may be used to implement an adaptive spread spectrum clock generator that automatically adjust PLL behavior when frequency is changed.

An alternative embodiment may provide adaptive spread spectrum capability by adjustment of a charge pump current. However, charge pump current may be more sensitive and/or more difficult to control than the gain of a VCO.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. An apparatus comprising:

a circuit configured to generate a spread spectrum clock signal, wherein said circuit comprises a voltage controlled oscillator having an automatically controlled gain.

2. The apparatus according to claim 1, wherein said gain is nonlinear.

3. The apparatus according to claim 1, wherein said gain varies in response to a frequency of said spread spectrum clock signal.

4. The apparatus according to claim 2, wherein a function curve for said nonlinear gain is generated according to predetermined criteria.

5. The apparatus according to claim 4, wherein said function curve is a parabolic curve.

6. The apparatus according to claim 4, wherein said function is a second degree or higher polynomial.

7. The apparatus according to claim 4, wherein a computer program is used to generate said function curve for said gain.

8. The apparatus according to claim 1, wherein said spread spectrum clock signal is generated in response to a reference signal having any frequency from 50 to 170 MHz.

9. The apparatus according to claim 1, wherein said circuit further comprises a single set of ROM codes.

10. The apparatus according to claim 9, wherein said ROM codes determine a frequency modulation profile for said spread spectrum clock signal.

11. The apparatus according to claim 10, wherein said circuit further comprises a divider circuit.

12. The apparatus according to claim 11, wherein said ROM codes control said divider circuit.

13. An apparatus comprising:

a voltage controlled oscillator (VCO) configured to generate an output signal in response to a control signal, wherein said VCO has a gain that is automatically controlled; and

a control circuit configured to generate said control signal in response to (i) a reference signal, (ii) said output signal, and (iii) a set of ROM codes.

14. A method for adapting a single spread spectrum ROM code to generate a spread spectrum clock signal over a wide continuous range of frequencies comprising the steps of:

(A) determining a nonlinear gain function for a voltage controlled oscillator (VCO) according to predetermined criteria; and

(B) adjusting a gain of said VCO according to said gain function in response to changes in frequency of an input signal.

15. The method according to claim 14, wherein step A comprises the sub-steps of:

(A-1) selecting a target frequency for said VCO;

(A-2) setting a gain value for said VCO;

(A-3) simulating a spread spectrum phase lock loop for a number of modulation cycles; and

(A-4) calculating an accumulated error deviation from an ideal modulation profile.

16. The method according to claim 15, further comprising the sub-step of:

(A-5) repeating steps A-2 through A-4 for a range of gains.

17. The method according to claim 16, further comprising the sub-step of:

(A-6) repeating steps A-1 through A-5 for a range of frequencies.

18. A computer readable media comprising instructions for performing the sub-steps according to claim 15.

19. A computer readable media comprising instructions for performing the sub-steps according to claim 16.

20. A computer readable media comprising instructions for performing the sub-steps according to claim 17.

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ABSTRACT OF THE DISCLOSURE

An apparatus comprising a circuit configured to generate a spread spectrum clock signal. The circuit may comprise a voltage controlled oscillator with a gain that may be automatically controlled.

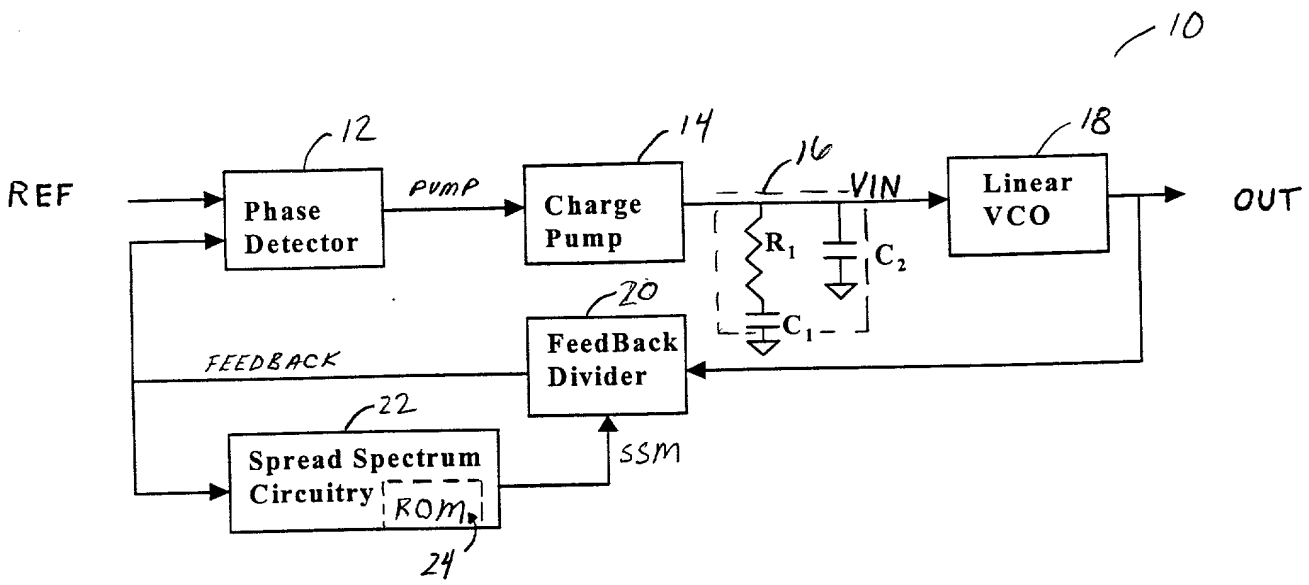

10
REF
12
Phase Detector
PUMP
14
Charge Pump
16
VIN
18
Linear VCO
OUT
R1
C2
C1
20
FeedBack Divider
FEEDBACK
22
Spread Spectrum Circuitry
ROM
24
SSM

FIG.1

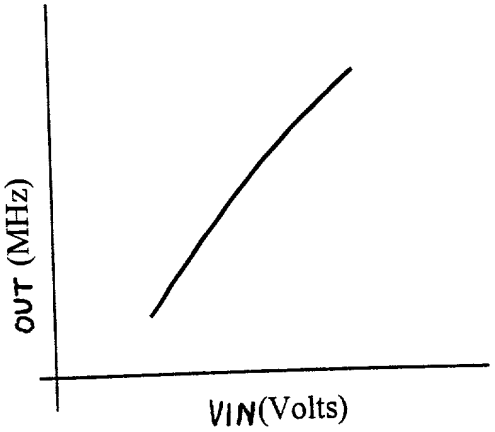

OUT (MHz)
VIN(Volts)

FIG.2

FIG.3a

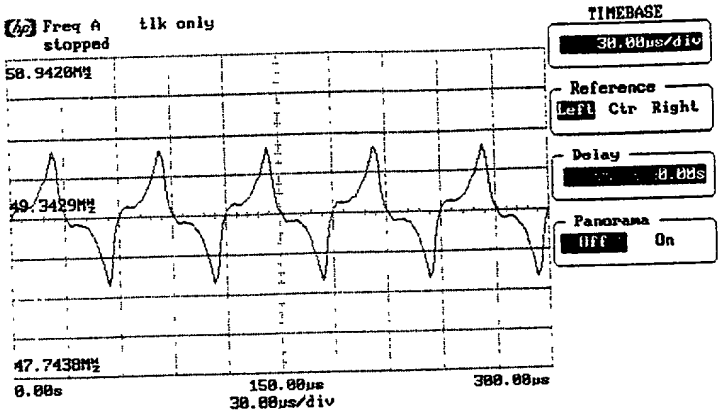


FIG.3b

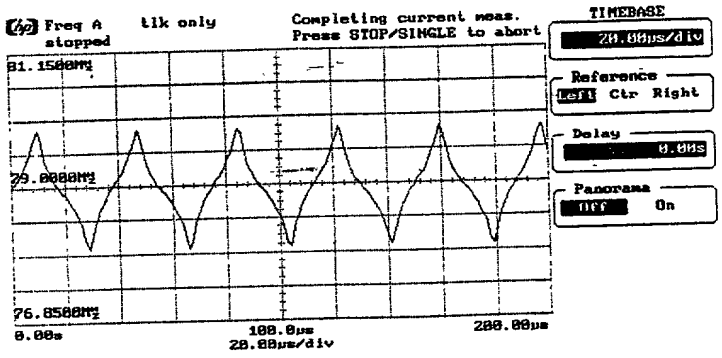


FIG.3c

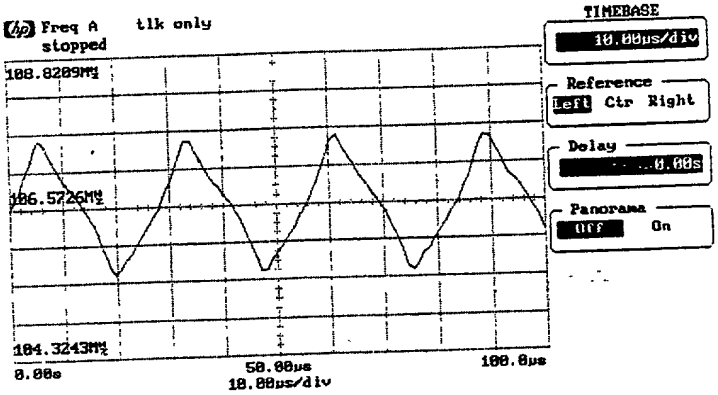
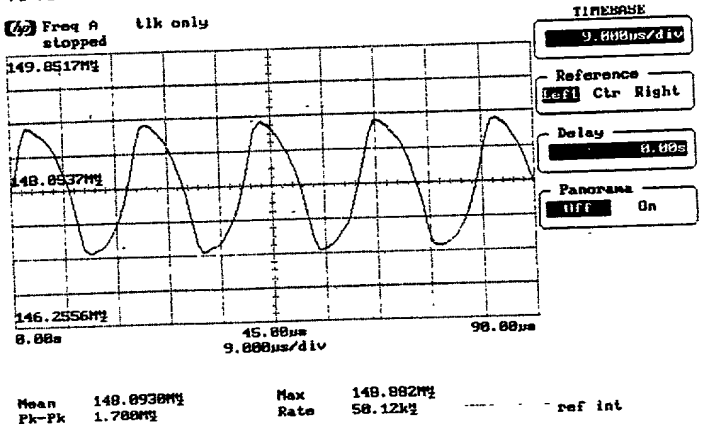


FIG.3d



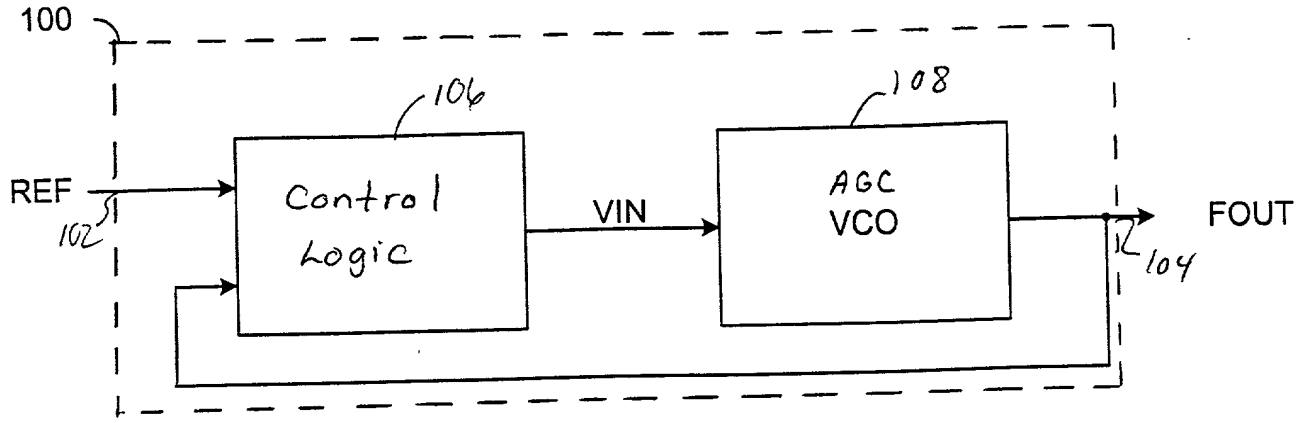

100
106
108
REF
102
Control Logic
VIN
AGC VCO
FOUT
104

FIG. 4

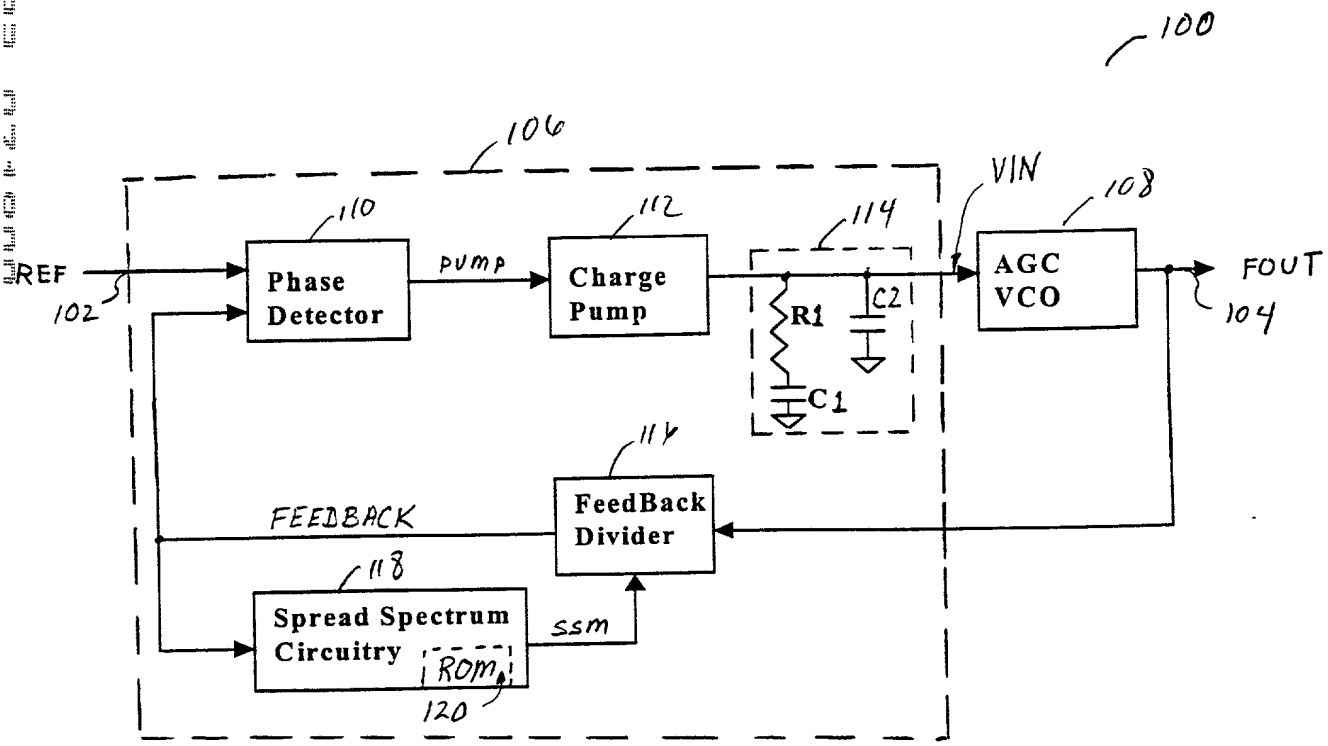

100
106
VIN
108
110
112
114
REF
102
Phase Detector
PUMP
Charge Pump
R1
C2
C1
AGC VCO
FOUT
104
116
FEEDBACK
FeedBack Divider
118
Spread Spectrum Circuitry
ROM
120
ssm

FIG.5

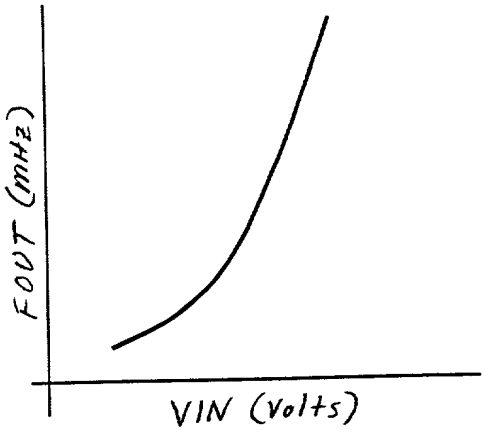

FOUT (mHz)
VIN (Volts)

FIG.6

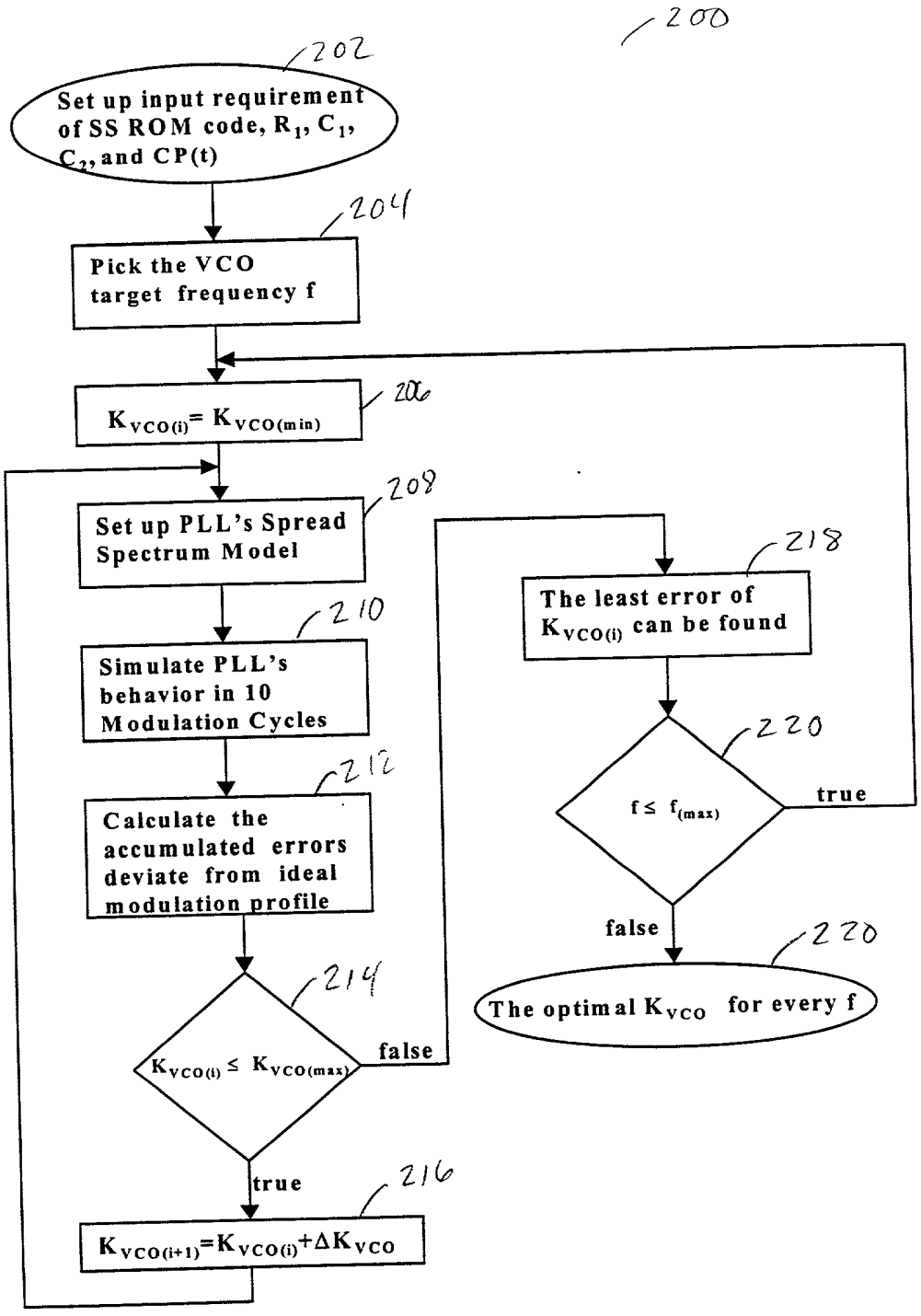

200
202
Set up input requirement of SS ROM code, R_1, C_1, C_2, and CP(t)
204
Pick the VCO target frequency f
206
$K_{VCO(i)} = K_{VCO(min)}$
208
Set up PLL's Spread Spectrum Model
210
Simulate PLL's behavior in 10 Modulation Cycles
212
Calculate the accumulated errors deviate from ideal modulation profile
214
$K_{VCO(i)} \leq K_{VCO(max)}$
false
true
216
$K_{VCO(i+1)} = K_{VCO(i)} + \Delta K_{VCO}$
218
The least error of $K_{VCO(i)}$ can be found
220
$f \leq f_{(max)}$
true
false
220
The optimal K_{VCO} for every f

FIG.7

FIG.8a

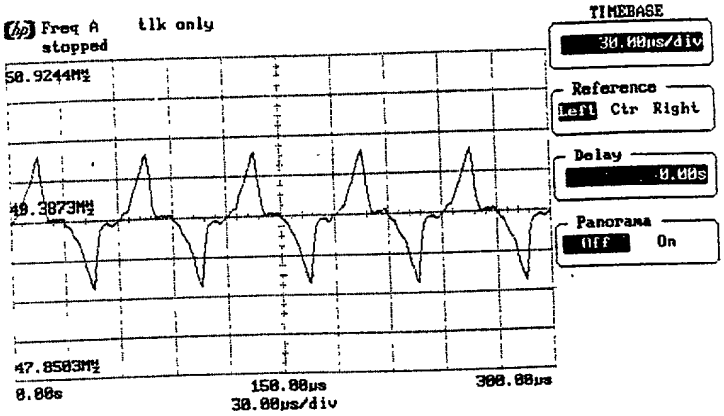


FIG.8b

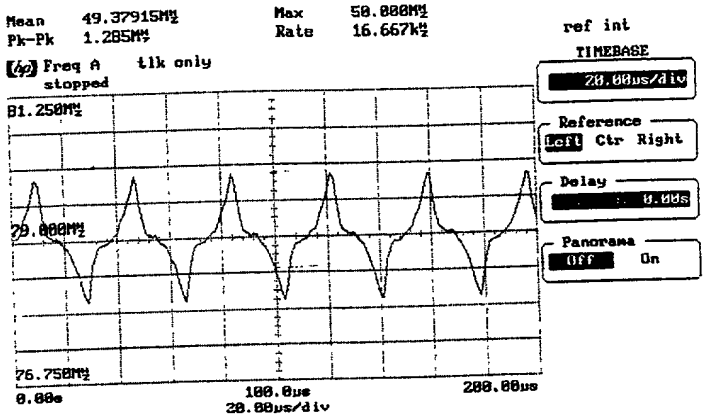


FIG.8c

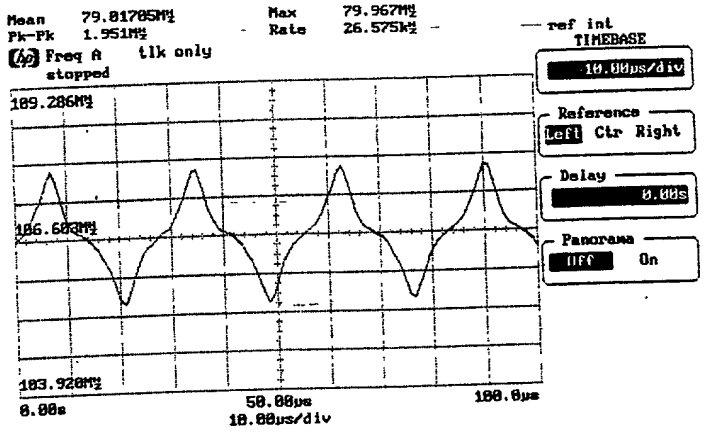
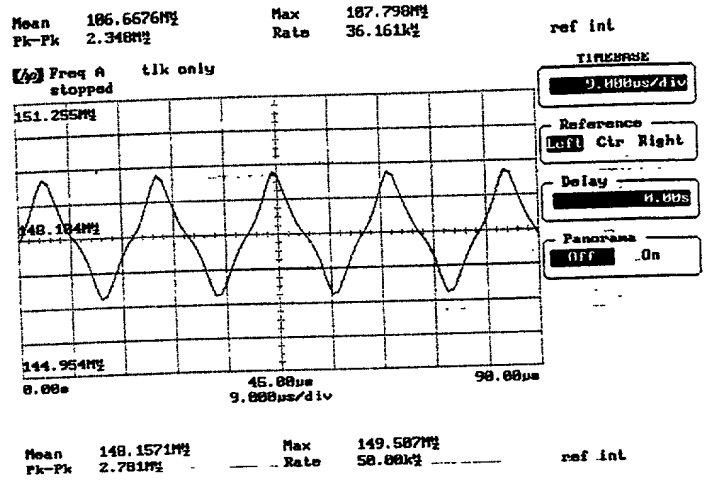


FIG.8d



Docket No. 0325.00377

DECLARATION, POWER OF ATTORNEY AND PETITION

We, the undersigned inventors, hereby declare that:

My residence, post office address and citizenship are given next to my name;

We believe that we are the first, original and joint inventors of the subject matter claimed in the application for patent entitled "**ADAPTIVE SPREAD SPECTRUM**", which:

__X__ is submitted herewith;

_____ was filed on _____ as Application Serial No. _____ and amended on _____;

We have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

We acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. We also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

> compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or
>
> refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

We hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.	Filing Date

We hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.	Filing Date	Status

JC542 U.S. PTO
09/618622
07/18/00

We hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.	Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, we acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

We hereby appoint as our attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

21363

PATENT TRADEMARK OFFICE

We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

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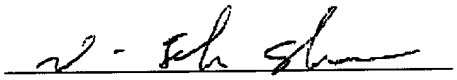
Name of First Joint Inventor



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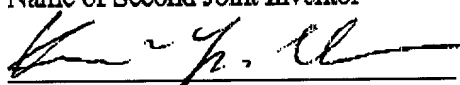

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